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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/699,321 | 10/31/2003 | Stewart Logie | 10069/26 | 2545 |

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| EXAMINER | |
|---|---|
| FENTY, JESSE A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,321 | LOGIE, STEWART | |
| | Examiner | Art Unit | |
| | Jesse A. Fenty | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *4-7,11,12 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 12* is/are allowed.

6)☒ Claim(s) *4-7,22,24 and 25* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

a. In re claim 7, neither the specification nor the drawings disclose how the gate electrode is electrically coupled to the substrate.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 4, 6, 7, 22, 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo et al. (US 2005/0035410 A1).

In re claim 4, Yeo (esp. Figs. 4, 6) discloses a semiconductor device, comprising:

a substrate having a first junction region (108) separated from a second junction region (106), wherein the substrate region is defined by a uniformly doped region extending from the first junction region to the second junction region;

a MOS gate electrode (120, 122) overlying the substrate region and separated therefrom by a gate oxide layer (114);

dielectric sidewall spacers (136) adjacent to opposing sides of the MOS gate electrode and overlying the uniformly doped substrate region;

wherein the first junction region comprises an anode and the second junction region comprises a cathode, and wherein the anode and the cathode have an opposite conductivity type.

In re claim 6, Yeo discloses the device of claim 4. The limitation, "wherein ... configurable ... regions" is a recitation of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 7, as best understood, Yeo discloses the device of claim 4, wherein the gate electrode is electrically coupled to the substrate.

In re claim 22, Yeo (esp. Figs. 4, 6) discloses a semiconductor device, comprising:

a MOS circuit coupled to a voltage supply node and a ground node (section [0027]); and

a lateral high voltage junction device for over voltage protection of the MOS circuit, the device coupled to the voltage supply and ground node in parallel with the MOS circuit, the device comprising:

a substrate having a first junction region (108) separated from a second junction region (106) by a uniformly doped substrate region extending from the first junction region to the second junction region;

an MOS gate electrode (122, 120) overlying the uniformly doped substrate region and separated therefrom by a gate oxide layer (114); and

dielectric sidewall spacers (136) adjacent to opposing sides of the MOS gate electrode and overlying the uniformly doped substrate region.

In re claim 24, Yeo discloses the device of claim 22, wherein the first junction region and the substrate region comprise semiconductor materials of different conductivity types, the first junction being coupled to the voltage supply node, and the second junction and the substrate region comprise a semiconductor material of the same conductivity types, the second junction being coupled to the ground node.

In re claim 25, Yeo discloses the device of claim 22, wherein the first junction region comprises an anode and the second junction region comprises a cathode, and wherein the anode and the cathode have an opposite conductivity type.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. (as above).

In re claim 5, Yeo discloses the device of claim 4, wherein the disclosure acknowledges the distance of the current path as a necessary variable in the determination of the size of the diode, but does not expressly disclose the optimum distance being 200nm or less. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a channel length of 200nm or less, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F. 2c 272, 205 USPQ 215 (CCPA 1980).

### *Allowable Subject Matter*

7. Claims 11 and 12 are allowed.

8. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The semiconductor device comprising at least a transistor coupled to the voltage supply node and to the ground node in parallel with the MOS circuit and a compensating diode coupled to the voltage supply ode and to the ground node in parallel with the MOS circuit and the transistor is neither anticipated nor obvious over the prior art of record.

### *Response to Arguments*

10. Applicant's arguments with respect to claims 4-7, 11-13 and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER